Abstracts

Very Low Power Gigabit Logic Circuits with Enhancement-Mode GaAs MESFETs

M. Ohmori, T. Mizutani and N. Kato. "Very Low Power Gigabit Logic Circuits with Enhancement-Mode GaAs MESFETs." 1981 MTT-S International Microwave Symposium Digest 81.1 (1981 [MWSYM]): 188-190.

Ultra high-speed enhemcement-mode GaAs MESFET integrated circuits, 0.6 µm in gate length, were fabricated using electron beam direct writing and employing recessed gate structure. The minimum delay time was 28.7 ps per gate with 2.3 mW power dissipation. At liquid nitrogen temperature, 77 K, the delay time was reduced to 17.5 ps with 9.2 mW power dissipation. A divide-by-eight counter was successfully demonstrated at 3.8 GHz with a power consumption of 23.6 mW per chip or 1.2 mW per gate.

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